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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/748,256	12/27/00	CHEN H	YO999-153DIV

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EXAMINER	
NADAV,O	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 08/14/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
09/748,256	Chen et al.
Examiner	**Art Unit**
ORI NADAV	2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Jun 29, 2001* .

2a) ☒ This action is **FINAL.** 2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *29-45* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *29-45* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☐ Notice of References Cited (PTO-892)
16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
18) ☐ Interview Summary (PTO-413) Paper No(s). _____
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claim 40 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The specification describes an amorphous silicon layer being converted to silicon layer, and STI's formed in the converted silicon layer. The text of the specification recites modifying the invention by using a SiGe epitaxial process to form islands with SiGe. There is no support in the text of the specification for a crystalized silicon layer formed by annealing a SiGe and having isolation trenches formed therein so as to remove defective regions, as recited in claim 28, in such a way as to enable one skilled in the art to which it pertains, or to make and/or use the device

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 29-45, insofar as in compliance with 35 U.S.C. 112, rejected under 35 U.S.C. 103(a) as being unpatentable over Witek et al. (6,146,970).

Witek et al. teach in figure 14 a substrate for mixed logic and memory applications comprising a bulk silicon region, and an SOI region (column 6, lines 9-10) comprising a single crystal silicon, an amorphous silicon layer 206 (column 6, lines 23-25) formed over the oxide layer, and islands of crystal silicon form STI's 210 formed at predetermined locations to remove defects on the SOI region, wherein a memory device is positioned in the bulk silicon region.

Regarding the processing limitations of forming a crystalized silicon layer by annealing amorphous silicon and a SiGe, and crystalizing the amorphous silicon using an exposed portion of the silicon as a seed and using STI's to remove defects on the SOI region, as recited in claims 29, 41, 45, 40 and 32, these would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced. In re Thorpe, 227 USPQ 964 (Fed. Cir. 1985). Therefore, the claimed structure is considered to be in at least obvious over Witek et al.' structure.

Regarding claim 35, Witek et al. teach in figure 22 a planarized upper surface of the STI's, the substrate and the silicon layer. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to planarize the upper surface of the device of figure 14 in order to improve the processing steps of the device.

Regarding claim 36, Witek et al. teach a crystal silicon having a crystal orientation which follows an underlying substrate, because the two materials are identical.

Regarding claims 38-39, it would have been obvious to a person of ordinary skill in the art at the time the invention was made form various types of memory and logic devices on the silicon bulk of is positioned in the bulk silicon region of Witek et al.'s device in order to use the device in a particular application.

5. Claims 29-45, insofar as in compliance with 35 U.S.C. 112, rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. (5,767,549).

Regarding claim 40, Chen et al. teach in figure 1 a substrate for mixed logic and memory applications comprising a bulk silicon region, and an SOI region 14 comprising a single crystal silicon, an SiGe layer 18 (column 2, line 65) formed over the oxide layer, and islands of crystal silicon form STI's 38 formed at predetermined locations to

remove defects on the SOI region, wherein a memory device is positioned in the bulk silicon region.

Regarding the processing limitations of forming a crystalized silicon layer by annealing amorphous silicon and a SiGe, crystalizing the amorphous silicon using an exposed portion of the silicon as a seed and using STI's to remove defects on the SOI region as recited in claims 29, 41, 45, 40 and 32, these would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced. In re Thorpe, 227 USPQ 964 (Fed. Cir. 1985). Therefore, the claimed structure is considered to be in at least obvious over Chen et al.' structure.

Regarding claims 29, 41 and 45, although Chen et al. do not teach an amorphous silicon layer formed on the silicon substrate, this is a processing limitation, since the amorphous silicon layer is later converted to crystal silicon.

Regarding claim 35, Chen et al. teach a planarized upper surface of the STI's, the substrate and the silicon layer. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to planarize the upper surface of the device of figure 14 in order to improve the processing steps of the device.

Regarding claim 36, Chen et al. teach a crystal silicon having a crystal orientation which follows an underlying substrate, because the two materials are identical.

Regarding claims 38-39, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to form various types of memory and logic devices on the silicon bulk of is positioned in the bulk silicon region of Chen et al.'s device in order to use the device in a particular application.

6. Claims 29-45, insofar as in compliance with 35 U.S.C. 112, rejected under 35 U.S.C. 103(a) as being unpatentable over Tsuchiaki (6,051,509).

Regarding claim 40, Tsuchiaki teaches in figure 6b a substrate for mixed logic and memory applications comprising a bulk silicon region, and an SOI region comprising a single crystal silicon, an SiGe layer (column 21, line 17) formed over the oxide layer, and STI's 201 formed at predetermined locations to remove defects on the SOI region, wherein the SiGe layer is at least partially positioned on a bulk region of the substrate and the SOI portion of the substrate.

Regarding the processing limitations of forming a crystalized silicon layer by annealing amorphous silicon and a SiGe, crystalizing the amorphous silicon using an exposed portion of the silicon as a seed and using STI's to remove defects on the SOI region as recited in claims 29, 41, 45, 40 and 32, these would not carry patentable weight in this

claim drawn to a structure, because distinct structure is not necessarily produced. In re Thorpe, 227 USPQ 964 (Fed. Cir. 1985). Therefore, the claimed structure is considered to be in at least obvious over Tsuchiaki's structure.

Regarding claims 29, 41 and 45, although Tsuchiaki does not teach an amorphous silicon layer formed on the silicon substrate, this is a processing limitation, since the amorphous silicon layer is later converted to crystal silicon.

Regarding claim 35, Tsuchiaki teaches a planarized upper surface of the STI's, the substrate and the silicon layer. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to planarize the upper surface of the device of figure 14 in order to improve the processing steps of the device.

Regarding claim 36, Tsuchiaki teaches a crystal silicon having a crystal orientation which follows an underlying substrate, because the two materials are identical.

Regarding claims 38-39, it would have been obvious to a person of ordinary skill in the art at the time the invention was made form various types of memory and logic devices on the silicon bulk of is positioned in the bulk silicon region of Tsuchiaki's device in order to use the device in a particular application.

Response to Arguments

7. Applicant argues on pages 6-8 that prior art does not teach the claimed method of making the device.

The examiner did not state that prior art teaches the claimed method of making the device. Claims 29-45 are directed to a semiconductor device and not to methods of making the device. Applicant does not claim the method of making the device.

8. Applicant argues on page 7 that layer 206 of Witek is formed over bulk silicon 202 and not over an insulator layer.

Witek et al. teach in column 6, lines 9-10 bulk silicon 202 comprises SOI. Therefore, Witek et al. teach layer 206 being formed over an insulator layer, as claimed.

9. Applicant argues on page 8 that Chen et al. do not teach a bulk silicon region and an SOI region 14

Chen et al. teach in figure 1 a bulk silicon region and an SOI region 14, as claimed.

10. Applicant argues on page 9 that the examiner is "completely and utterly incorrect", because conventional processes do not result in a completely buried insulator layer, which in turn is completely surrounded with crystalized silicon.

Note that the above features are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

11. Applicant argues on page 10 that the specification "completely and unambiguously explains, for example, how SiGe epitaxial process can be used to form the claimed device".

The examiner would like applicant to point out exactly where in the specification it is completely and unambiguously explained how SiGe epitaxial process can be used to form the claimed device.

Conclusion

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722

and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(703) 308-8138**. The Examiner is in the Office generally between the hours of 7 AM to 3 PM (Eastern Standard Time) Monday through Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached at **(703) 308-2772.**

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER

Ori Nadav

August 10, 2001